Attorney Docket Number 00303.326US1

SILICON CARBIDE GATE TRANSISTOR AND FABRICATION PROCESS

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Field of the Invention

The present invention relates generally to integrated circuits, and particularly to a silicon carbide gate field-effect transistor and complementary metal-oxide-semiconductor (CMOS) compatible method of fabrication.

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Background of the Invention

Field-effect transistors (FETs) are typically produced using a standard complementary metal-oxide-semiconductor (CMOS) integrated circuit fabrication process. As well known in the art, such a process allows a high degree of integration

15 such that a high circuit density can be obtained with relatively few well-established masking and processing steps. A standard CMOS process is typically used to fabricate FETs that each have a gate electrode that is composed of n-type conductively doped polycrystalline silicon (polysilicon) material.

The intrinsic properties of the polysilicon gate material affects operating

20 characteristics of the FET that is fabricated using a standard CMOS process. Silicon (monocrystalline and polycrystalline) has intrinsic properties that include a relatively small energy band gap (E_g), e.g. approximately 1.2 Volts, and a corresponding electron affinity (χ) that is relatively large, e.g. $\chi \approx 4.2$ eV. For example, for p-channel FETs fabricated by a typical CMOS process, these and other material properties result in a

25 large turn-on threshold voltage (V_T) magnitude. As a result, the V_T magnitude must be downwardly adjusted by doping the channel region that underlies the gate electrode of the FET. Doping to adjust the V_T magnitude typically includes the ion-implantation of acceptor dopants, such as boron, through the polysilicon gate material and an underlying gate insulator into the channel region of the underlying silicon substrate. A typical V_T

magnitude of approximately 0.7 Volts results from the ion-implantation adjustment step.

One drawback of polysilicon gate FETs is that the V_T magnitude adjustment by ion-implantation is particularly difficult to carry out in semiconductor-on-insulator

5   (SOI) and other thin film transistor technology. In SOI technology, the FET channel region is formed in a semiconductor layer that is formed upon an insulating region of the substrate. The semiconductor layer may be only 1000Å thick, making it difficult to obtain a sufficiently sharply defined dopant distribution through ion-implantation.

Another drawback of polysilicon gate FETs is that their intrinsic characteristics

10   are likely to change during subsequent high temperature process steps. For example, the polysilicon gate is typically doped with boron impurities that have a high diffusivity in polysilicon. Because of this high diffusion rate, the boron impurities that are introduced into the polysilicon gate electrode of the FET diffuse through the underlying gate oxide during subsequent high temperature processing steps. As a result, the V_T

15   magnitude the FETs may change during these subsequent high temperature processing steps.

For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a transistor having an even lower V_T

20   magnitude, in order to operate at lower power supply voltages. There is an additional need in the art to obtain such lower V_T magnitudes without using ion-implantation, particularly for thin film transistor devices in a SOI process. There is a further need in the art to obtain V_T magnitudes that remain stable in spite of subsequent thermal processing steps.

25   Halvis et al. (U.S. Patent Number 5,369,040) discloses a charge-coupled device (CCD) photodetector which has transparent gate MOS imaging transistors fabricated from polysilicon with the addition of up to 50% carbon, and preferably about 10% carbon, which makes the gate material more transparent to the visible portion of the energy spectrum. However, the Halvis et al. patent is directed to improving gate

transmissivity to allow a greater portion of incident light in the visible spectrum to penetrate the gate. Halvis et al. did not recognize the need to improve the gate characteristics of FETs by lowering V_T magnitudes or stabilizing V_T magnitudes over subsequent thermal processing steps. Halvis et al. does not disclose or suggest the use

5   of carbon in a field-effect transistor gate in the absence of incident light. Thus, the above described needs are unresolved in the art of fabrication of FETs using CMOS processes.

Summary of the Invention

10   One aspect of the present invention provides a field-effect transistor (FET) having an electrically interconnected gate formed of polycrystalline or microcrystalline silicon carbide (SiC) material. The SiC gate material has a lower electron affinity and a higher work function than a polysilicon gate material. The characteristics of the SiC gate FET include a lower threshold voltage (V_T) magnitude and a lower tunneling

15   barrier voltage as compared to polysilicon gate FETs.

Another aspect of the invention provides a method for fabricating a transistor including an electrically interconnected SiC gate. Source and drain regions are fabricated in a silicon substrate, separated from each other and defining a channel region therebetween. An insulating region is fabricated over the channel region. A SiC gate is

20   fabricated over the insulating region. In one embodiment, SiC gate fabrication includes depositing an SiC layer on the insulating region using low pressure chemical vapor deposition (LPCVD) and etching the SiC material to a desired pattern using a reactive ion etch (RIE) process.

The invention provides numerous advantages. For example, the SiC gate FET

25   provides lower V_T magnitudes, allowing integrated circuit operation at lower power supply voltages. The lower power supply voltage, in turn, provides advantages including lower power consumption and ease in downward scaling of transistor dimensions without unacceptably increasing electric fields. The lower V_T magnitudes also enable higher switching speeds and improved performance. The SiC gate FET also

provides lower V_T magnitudes without adjustment by ion-implantation. This is particularly useful for semiconductor-on-insulator (SOI) and other thin film transistor devices in which an adequately sharply defined dopant distribution is difficult to obtain by ion-implantation V_T adjustment. The SiC gate FET also provides V_T magnitudes that

5   are stable in spite of subsequent thermal processing steps. The SiC gate FET further provides more optimal V_T magnitudes for n-channel FETs (e.g., enhancement rather than depletion mode).

Brief Description of the Drawings

10   In the drawings, like numerals describe substantially similar components throughout the several views.

FIG. **1** is a cross-sectional view, illustrating generally one embodiment of a transistor according to one aspect of the invention, including a silicon carbide (SiC) gate.

15   FIG. **2** is a graph, illustrating generally barrier height versus tunneling distance for a SiC gate transistor.

FIGS. **3A-3H** illustrate generally examples of process steps for fabricating n-channel and p-channel SiC gate transistors.

FIG. **4** is a simplified block diagram, illustrating generally one embodiment of a

20   semiconductor memory device incorporating SiC gate transistors.

Detailed Description of the Invention

In the following detailed description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in which is shown,

25   by way of illustration, a specific embodiment in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. This embodiment is described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural and electrical changes may be made without departing from the scope of the present

invention. The terms wafer and substrate used in the following description include any semiconductor-based structure having an exposed surface with which to form the integrated circuit structure of the invention. Wafer and substrate are used interchangeably to refer to semiconductor structures during processing, and may include

5   other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended

10   claims.

The present invention discloses a field-effect transistor (FET) having gate that is formed of a polycrystalline or microcrystalline silicon carbide (SiC) material, which includes any material that incorporates both silicon and carbon into the gate region of a FET. The SiC gate FET includes characteristics such as, for example, a lower electron

15   affinity and a higher work function than a conventional polycrystalline silicon (polysilicon) gate FET. In one embodiment, the FET gate is electrically interconnected or otherwise driven by an input signal. The SiC gate FET provides lower threshold voltage (V_T) magnitudes, allowing operation at lower power supply voltages. This, in turn, allows lower power consumption, and facilitates the downward scaling of

20   transistor dimensions without increasing electric fields unacceptably. The lower V_T magnitudes also enables higher switching speeds and improved performance. The SiC gate FET also provides lower V_T magnitudes without adjustment by ion-implantation. This is particularly useful for semiconductor-on-insulator (SOI) and other thin film transistor devices in which a sufficiently sharp doping profile is difficult to obtain by

25   ion-implantation. The SiC gate FET also includes V_T magnitudes that are stable in spite of subsequent thermal processing steps. The SiC gate FET further provides more optimal threshold voltage magnitudes for n-channel FETs (e.g., enhancement rather than depletion mode). In another embodiment, the SiC gate FET further provides floating gate transistors having lower tunneling barriers, such as described in Forbes

U.S. patent ~~application serial number 08/790,603~~ number 5,801,401 issued September 1, 1998, and entitled "Flash Memory with Microcrystalline Silicon Carbide Film Floating Gate," which is assigned to the assignee of the present application and which is herein incorporated by reference. This allows faster storage and removal of charge from the floating gates, and is particularly useful

5 for speeding erasing and writing operations in flash electrically erasable and programmable read-only memories (EEPROMs) and other applications.

FIG. 1 is a cross-sectional view illustrating generally, by way of example, one embodiment of a n-channel FET provided by the invention. The FET includes a source region 102, a drain region 104 and a gate region 106. In one embodiment, source 102

10 and drain 104 are fabricated by forming ~~regions of~~ highly doped (n+) regions in a lightly doped (p-) silicon semiconductor substrate 108. In another embodiment, substrate 108 includes a thin semiconductor surface layer formed on an underlying insulating portion, such as in a SOI or other thin film transistor process technology. Source 102 and drain 104 are separated by a predetermined length in which a channel

15 region 110 is formed.

According to one aspect of the invention, gate 106 is formed of SiC material. The silicon carbide material forming gate 106 is described more generally as Si_xC_y. In one embodiment, the SiC gate material is approximately stoichiometric, i.e., $x \approx 0.5$. However, other embodiments of the invention could include less carbon, i.e., $x < 0.5$, or

20 more carbon, i.e., $x > 0.5$. For example, but not by way of limitation, one embodiment of the SiC gate material is illustrated by $0.1 < x < 0.5$. Another example embodiment is illustrated by way of example, but not by way of limitation, by $0.4 < x < 0.6$. According to one aspect of the invention, the SiC gate material can include either or both polycrystalline or microcrystalline embodiments of the SiC gate material.

25 In one embodiment, an insulating layer, such as silicon dioxide (oxide) 114 or other insulating layer, is formed by chemical vapor deposition (CVD). Oxide 114 isolates gate 106 from other layers, such as layer 112. In another embodiment, gate 106 is oxidized to form at least a portion of oxide 114 to isolate gate 106 from other layers such as layer 112. In one embodiment, for example, layer 112 is a polysilicon control

gate in a floating gate transistor in an electrically erasable and programmable read-only memory (EEPROM) memory cell. In this embodiment, gate **106** is floating (electrically isolated) for charge storage thereupon, such as by known EEPROM techniques. In another embodiment such as, for example, a driven gate embodiment in which gate **106**

5 is electrically interconnected, layer **112** is a metal or other conductive interconnection line that is located above gate **106**.

The upper layers, such as layer **112** can be covered with a layer **116** of a suitable insulating material in the conventional manner, such as for isolating and protecting the physical integrity of the underlying features. Gate **106** is isolated from channel **110** by

10 an insulating layer such as thin oxide layer **118**, or any other suitable dielectric material. In one embodiment, thin oxide layer **118** is a gate oxide layer that can be approximately 100 angstroms (Å) thick, such as for conventional FET operation. In another embodiment, such as in a floating gate transistor, thin oxide layer **118** is a tunnel oxide material that can be approximately 50 - 100 Å thick.

15 The SiC gate **106** has particular advantages over polysilicon gates used in FETs fabricated using a conventional complementary metal-oxide-semiconductor (CMOS) process due to different characteristics of the SiC material. For example, SiC is a wide bandgap semiconductor material with a bandgap energy of about 2.1 eV, in contrast to silicon (monocrystalline or polycrystalline), which has a bandgap energy of about 1.2

20 eV. Moreover, SiC has an electron affinity of about 3.7 to 3.8 eV, in contrast to silicon, which has an electron affinity of about 4.2 eV. The smaller electron affinity of the SiC gate **106** material reduces the barrier potential at the interface between gate **106** and thin oxide layer **118**. In an embodiment in which thin oxide layer **118** is a tunnel oxide in a floating gate transistor EEPROM memory cell, the lower electron affinity of SiC

25 reduces the tunneling distance and increases the tunneling probability. This speeds the write and erase operations of storing and removing charge by Fowler-Nordheim tunneling to and from the gate **106**, which is a floating gate. This is particularly advantageous for "flash" EEPROMs in which many floating gate transistor memory cells must be erased simultaneously. The large charge that must be transported by

Fowler-Nordheim tunneling during the erasure of a flash EEPROM typically results in relatively long erasure times. By reducing the tunneling distance and increasing the tunneling probability, the SiC gate **106** reduces erasure times in flash EEPROMs.

P-type SiC also has a larger work function than polysilicon, providing other

5   advantages for a FET having a SiC gate **106**, particularly in an electrically interconnected or driven gate embodiment of the present invention. For example, large work function gates provide advantages for FETs fabricated using SOI starting material and process technology. In an SOI process, p-channel polysilicon gate FETs typically operate as fully depleted thin film transistor devices and require V_T magnitude

10   adjustment by ion-implantation. However, such ion-implantation adjustment is difficult because the semiconductor layer may be only 1000Å thick, making it difficult to obtain a sufficiently sharply defined dopant distribution through ion-implantation. The p-type SiC gate, however, has a larger work function than polysilicon, thereby providing reduced V_T magnitudes for p-channel FETs without adjustment by ion-implantation.

15   The reduced V_T magnitudes of the p-channel FETs advantageously allows operation at lower power supply voltages. This, in turn, lowers power consumption and facilitates the downward scaling of FET dimensions without increasing electric fields unacceptably. The reduced V_T magnitudes also enable higher switching speeds and improved integrated circuit performance. Furthermore, the V_T magnitudes obtained

20   according to the present invention are stable in spite of subsequent thermal processing steps, since no migratory dopants are ion-implanted to adjust the p-channel V_T magnitude. Such lower V_T magnitudes and accompanying advantages are difficult to achieve by other integrated circuit manufacturing techniques.

Large work function p-type SiC gates also provide advantages for n-channel

25   FETs. For example, while polysilicon gate FETs tend to result in depletion mode n-channel V_T magnitudes, p-type SiC gates more easily provide enhancement mode operation, which is often a more desirable device characteristic for designing integrated circuits.

FIG. **2** illustrates generally how the smaller electron affinity provides a smaller barrier potential. The smaller barrier potential reduces the distance that electrons stored on the gate have to traverse by Fowler-Nordheim tunneling to be stored upon or removed from the polycrystalline or microcrystalline SiC gate **106**. The reduced

5 tunneling distance allows easier charge transfer, such as during writing or erasing data in a floating gate transistor in a flash EEPROM memory cell. In FIG. **2**, "do" represents the tunneling distance of a typical polysilicon floating gate transistor due to the barrier height represented by the dashed line "OLD". The tunneling distance "dn" corresponds to a SiC gate and its smaller barrier height represented by the dashed line "NEW". Even

10 a small reduction in the tunneling distance results in a large increase in the tunneling probability, because the tunneling probability is an exponential function of the reciprocal of the tunneling distance. The increased tunneling probability of the SiC gate **106** advantageously provides faster programming and erasure times for SiC gate floating gate transistors in flash EEPROM memories. Flash EEPROM memories using

15 lower V_T magnitude SiC gate floating gate transistors also operate at lower power supply voltages, as described above.

The transistor of FIG. **1** illustrates generally, by way of example, an n-channel FET that includes an SiC gate. In one embodiment, for example, the transistor can be formed on substrate **108** using an n-well CMOS process, enabling monolithic CMOS

20 fabrication of n-channel and p-channel FETs on a common substrate. In one embodiment, both the n-channel and the p-channel FETs include a polycrystalline or microcrystalline SiC gate. Thus, with appropriate doping, the FET illustrated in FIG. 1 could also represent a p-channel FET. Applications of the p-channel and n-channel SiC gate FETs include any application in which conventionally formed polysilicon gate

25 FETs are used.

FIGS. **3A - 3H** illustrate generally examples of process steps for fabricating n-channel and p-channel SiC gate transistors according to the present invention. The n-channel and p-channel FETs can be produced on a silicon or other semiconductor

substrate, an SOI substrate, or any other suitable substrate **108**. Only the process steps that differ from conventional CMOS process technology are described in detail.

In FIG. **3A**, substrate **108** undergoes conventional CMOS processing up to the formation of the gate structure, including formation of field oxide 300 for defining

5   active regions 302, and the formation of well regions, such as n-well 304 in which p-channel transistors will be fabricated.

In FIG. **3B**, an insulating layer, such as thin oxide layer **118**, is formed on substrate **108**, such as by dry thermal oxidation, including over the portions of the active area regions **302** in which n-channel and p-channel FETs are formed. In one

10   embodiment, thin oxide layer **118** is a gate oxide layer that can be approximately 100 angstroms (Å) thick. In another embodiment, such as in a floating gate transistor, thin oxide layer **118** is a tunnel oxide material that can be approximately 50 - 100 Å thick.

In FIG. **3C**, a thin film **306** of conductively doped polycrystalline or microcrystalline SiC is then deposited, such as by chemical vapor deposition (CVD)

15   over the entire wafer, including over thin oxide layer **118**. The chemical composition of thin film **306** may be different for the particular deposition conditions of the polycrystalline and microcrystalline SiC, as illustrated by way of the particular examples described above.

Conventional FETs usually use n+ doped (e.g., phosphorus as dopant) gate

20   regions for both p-channel and n-channel FETs, even though p+ doped (e.g., boron as dopant) gate regions would provide more desirable operating characteristics. This is because boron easily diffuses out of the polysilicon gate regions during subsequent high temperature processing steps. By contrast, one aspect of the present invention is that it allows formation of n+ doped or p+ doped SiC gate regions. Since the diffusion rate of

25   the boron dopant is lower in SiC than in polysilicon, boron can be used as a dopant in the SiC gate material. Thus, one advantage of the present invention is that the V_T magnitudes in the SiC gate FETs are less affected by subsequent high temperature process steps than those of conventional polysilicon gate FETs. This allows greater control of the V_T magnitudes in the SiC gate FETs of the present invention.

In one embodiment, for example, SiC film **306** is deposited using low-pressure chemical vapor deposition (LPCVD), providing the structure illustrated in FIG. **3C**. The LPCVD process uses either a hot-wall reactor or a cold-wall reactor with a reactive gas, such as a mixture of $Si(CH_3)_4$ and Ar. Examples of such processes are disclosed in

5 an article by Y. Yamaguchi et al., entitled "Properties of Heteroepitaxial 3C-SiC Films Grown by LPCVD", in the 8th International Conference on Solid-State Sensors and Actuators and Eurosensors IX, Digest of Technical Papers, page 3. vol. (934+1030+85), pages 190-3, Vol. 2, 1995, and in an article by M. Andrieux, et al., entitled "Interface and Adhesion of PECVD SiC Based Films on Metals", in supplement Le Vide

10 Science,Technique et Applications. (France), No. 279, pages 212-214, 1996. However, SiC film **306** can be deposited using other techniques such as, for example, enhanced CVD techniques known to those skilled in the art including low pressure rapid thermal chemical vapor deposition (LP-RTCVD), or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy

15 (MBE). Other examples of forming SiC film **306** include reactive magnetron sputtering, DC plasma discharge, ion-beam assisted deposition, ion-beam synthesis of amorphous SiC films, laser crystallization of amorphous SiC, laser reactive ablation deposition, and epitaxial growth by vacuum anneal. The conductivity of the SiC film **306** can be changed by ion implantation during subsequent process steps, such as during

20 the self-aligned formation of source/drain regions for the n-channel and p-channel FETs.

In FIG. **3D**, SiC film **306** is patterned and etched, together with the underlying thin oxide layer **118**, to form SiC gate **106**. SiC film **306** is patterned using standard techniques and is etched using plasma etching, reactive ion etching (RIE) or a

25 combination of these or other suitable methods. For example, SiC film **306** can be etched by RIE in a distributed cyclotron resonance reactor using a SF_6/O_2 gas mixture using SiO_2 as a mask with a selectivity of 6.5. Such process is known in the art and is disclosed, for example, in an article by F. Lanois, entitled "Angle Etch Control for Silicon Power Devices", which appeared in Applied Physics Letters, Vol 69, No. 2,

pages 236-238, July 1996. Alternatively, SiC film **306** can be etched by RIE using the mixture SF_6 and O_2 and $F_2/Ar/O_2$. An example of such a process is disclosed in an article by N. J. Dartnell, et al., entitled "Reactive Ion Etching of Silicon Carbide" in Vacuum, Vol. 46, No. 4, pages 349-355, 1955. The etch rate of SiC film **306** can be

5   significantly increased by using magnetron enhanced RIE.

FIG. **3E** illustrates one embodiment in which SiC gate **106** is oxidized after formation, providing a thin layer **310** represented by the dashed line in FIG. **3E**. SiC gate **106** can be oxidized, for example, by plasma oxidation similar to reoxidation of polycrystalline silicon. During the oxidation process, the carbon is oxidized as carbon

10   monoxide or carbon dioxide and vaporizes, leaving the thin layer **310** of silicon oxide over SiC gate **106**. In one embodiment, thin layer **310** is used as, or as a portion of, an intergate dielectric between floating and control gates in a floating gate transistor embodiment of the present invention.

FIG. **3F** illustrates generally a self-aligned embodiment of the formation of n-

15   channel FET source/drain regions **312** and p-channel FET source/drain regions **314** for the p-channel FET. The doping of SiC gate **106** can be changed by ion implantation, such as during the formation of n-channel FET source/drain regions **312** or p-channel FET source/drain regions **314** for the p-channel FET. For example, a p-type SiC film **306** can be deposited, and its doping then changed to n+ by leaving SiC gate **106**

20   unmasked during the formation of the n+ source/drain regions **312** for the n-channel FET.

FIG. **3G** illustrates generally the formation of an insulating layer, such as oxide **114** or other suitable insulator, after formation of n-channel FET source/drain regions **312** and p-channel FET source/drain regions **314** for the p-channel FET. In one

25   embodiment, oxide **114** is deposited over the upper surface of the integrated circuit structure using a standard CVD process. Oxide **114** isolates SiC gate **106** from other gates such as, for example, an overlying control gate layer **112** where SiC gate **106** is a floating gate in a floating gate transistor EEPROM memory cell. Oxide **114** also isolates SiC gate **106** from any other conductive layer **112**, such as polysilicon layers,

gates, metal lines, etc., that are fabricated above and over SiC gate **106** during subsequent process steps. Insulating layer **116** is produced on the structure in a conventional manner.

FIG. **4** is a simplified block diagram illustrating generally one embodiment of a memory **400** system incorporating SiC gate FETs according to one aspect of the present invention. The SiC gate FETs are used in various applications within memory **400** including, for example, in logic and output driver circuits. The SiC gate FETs can also function as memory cell access FETs, such as in a dynamic random access memory (DRAM) embodiment of memory **400**, or as other memory elements therein. In one embodiment, memory **400** is a flash EEPROM, and the SiC gate FETs are floating gate transistors that are used for nonvolatile storage of data as charge on the SiC floating gates. However, the SiC gate FETs can also be used in other types of memory systems, including SDRAM, SLDRAM and RDRAM devices, or in programmable logic arrays (PLAs), or in any other application in which transistors are used.

FIG. **4** illustrates, by way of example but not by way of limitation, a flash EEPROM memory **400** comprising a memory array **402** of multiple memory cells. Row decoder **404** and column decoder **406** decode addresses provided on address lines **408** to access addressed SiC gate floating gate transistors in the memory cells in memory array **402**. Command and control circuitry **410** controls the operation of memory **400** in response to control signals received on control lines **416** from a processor **401** or other memory controller during read, write, and erase operations.

As described above, the floating SiC gates of the floating gate transistors in memory array **402** advantageously reduce the tunneling distance and increase the tunneling probabilities, thereby speeding write and erase operations of memory **400**. This is particularly advantageous for "flash" EEPROMs in which many floating gate transistor memory cells must be erased simultaneously, which normally results in relatively long erasure times. By reducing the tunneling distance and increasing the tunneling probability, charge is more easily transferred to and from the SiC floating gates, thereby reducing erasure times in flash EEPROMs.

Conclusion

Thus, the present invention provides a FET having a polycrystalline or microcrystalline SiC gate. The SiC gate FET characteristics include a lower electron affinity and higher work function than a conventional polysilicon gate FET. The SiC

5   gate FET provides lower V_T magnitudes, allowing operation at lower power supply voltages. This, in turn, lowers power consumption and facilitates downward scaling of transistor dimensions without increasing electric fields unacceptably. The lower V_T magnitudes also enable higher switching speeds and improved performance. The SiC gate FET also provides lower V_T magnitudes without adjustment by ion-implantation.

10 This aspect of the invention is particularly useful for SOI, thin film transistors, and any other devices in which ion-implantation may not yield a sufficiently sharp dopant distribution. The SiC gate FET provides V_T magnitudes that are stable in spite of subsequent thermal processing steps. The SiC gate FET also provides more optimal threshold voltage magnitudes for n-channel FETs (e.g., enhancement rather than

15 depletion mode). In one embodiment, the SiC gate FET has an electrically interconnected or driven gate. In another embodiment, the SiC gate FET further provides floating gate transistors that allow faster storage and erasure such as, for example, used in flash EEPROMs.

Although specific embodiments have been illustrated and described herein, those

20 of ordinary skill in the art will appreciate that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.